## AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A communications system comprising:

a decision feedback equalizer adapted to reduce channel related distortion in received data, wherein the decision feedback equalizer is configured to generate ~~generates~~ equalized data; and

a clock and data recovery circuit coupled to the decision feedback equalizer, ~~wherein~~ the clock and data recovery circuit configured to generate ~~generates~~ an extracted clock signal,

wherein the clock and data recovery circuit is configured to adjust a phase of the extracted clock signal relative to the equalized data ~~having an adjustable phase offset from the equalized data~~ to compensate for processing delays in the decision feedback equalizer, and

wherein the decision feedback equalizer includes a retimer that is configured to generate ~~generates~~ recovered equalized data from the equalized data in response to the extracted clock signal.

2. (Currently Amended) The communications system of claim 1 wherein the decision feedback equalizer comprises a summer that is configured to generate ~~generates~~ a combined signal by combining an equalized feedback signal with the received data to reduce the channel related distortion.

3. (Currently Amended) The communications system of claim 2 wherein the decision feedback equalizer further comprises a slicer coupled to the summer, wherein the slicer is configured to generate ~~generates~~ the equalized data by converting the combined signal to a binary signal and wherein the clock and data recovery circuit is configured to generate ~~generates~~ the extracted clock signal ~~having an adjustable phase offset~~ from the binary signal.

4. (Currently Amended) The communications system of claim 3 wherein the equalizer retimer comprises a flip flop coupled to the slicer and the clock and data recovery circuit, and wherein the flip flop is configured to generate ~~generates~~ recovered equalized data from the binary signal in response to the extracted clock signal.

5. (Currently Amended) The communications system of claim 1 wherein the clock and data recovery circuit comprises:

a phase detector configured to generate ~~for generating~~ a phase error signal in accordance with difference in phase of the extracted clock signal and the equalized data;

a voltage controlled oscillator configured to generate ~~for generating~~ the extracted clock signal as a function of the phase error signal; and

a delay coupled between the voltage control oscillator and the phase detector configured to adjust the ~~for adjusting~~ phase of the extracted clock signal.

6. (Currently Amended) The communications system of claim 1 wherein the clock and data recovery circuit comprises:

a phase detector configured to generate ~~for generating~~ a phase error signal in accordance with a difference in phase of the extracted clock signal and the equalized data; and

a voltage controlled oscillator configured to generate ~~for generating~~ the extracted clock signal as a function of the phase error signal,

wherein the phase detector is configured to adjust ~~adjusts~~ the phase error signal in response to a phase offset signal to adjust the phase of the extracted clock signal.

7. (Currently Amended) A communication system comprising:

a transmitter transmitting an information signal over a communication media; and

a receiver coupled to the communication media for receiving the transmitted information signal, wherein the receiver comprises:

a decision feedback equalizer adapted to reduce channel related distortion in received data, wherein the decision feedback equalizer is configured to generate ~~generates~~ equalized data; and

a clock and data recovery circuit coupled to the equalizer, ~~wherein~~ the clock and data recovery circuit configured to generate ~~generates~~ an extracted clock signal,

wherein the clock and data recovery circuit is configured to adjust a phase of the extracted clock signal relative to the equalized data ~~having an adjustable phase offset~~

~~from the equalized data~~ to compensate for processing delays in the decision feedback equalizer, and

wherein the decision feedback equalizer includes a retimer that is configured to generate ~~generates~~ recovered equalized data from the equalized data in response to the extracted clock signal.

8. (Currently Amended) The communications system of claim 7 wherein the decision feedback equalizer comprises a summer that is configured to generate ~~generates~~ a combined signal by combining an equalized feedback signal with the received data to reduce the channel related distortion.

9. (Currently Amended) The communications system of claim 8 wherein the decision feedback equalizer further comprises a slicer coupled to the summer, wherein the slicer is configured to generate ~~generates~~ the equalized data by converting the combined signal to a binary signal and wherein the clock and data recovery circuit is configured to generate ~~generates~~ the extracted clock signal ~~having an adjustable phase offset~~ from the binary signal.

10. (Currently Amended) The communications system of claim 9 wherein the equalizer retimer comprises a flip flop coupled to the slicer and the clock and data recovery circuit, and wherein the flip flop is configured to generate ~~generates~~ recovered equalized data from the binary signal in response to the extracted clock signal.

11. (Currently Amended) The communications system of claim 10 wherein the equalizer further comprises a multiplier coupled to the retimer and wherein the equalizer is configured to apply ~~applies~~ an equalization coefficient to the recovered equalized data to generate the equalized feedback signal.

12. (Currently Amended) A communications system comprising:

a decision feedback equalizer adapted to reduce channel related distortion in received data, the decision feedback equalizer comprising:

a summer that is configured to combine ~~combines~~ an equalized feedback signal with the received data,

a slicer coupled to the summer, ~~wherein~~ the slicer being configured to convert ~~converts~~ the combined signal to a binary signal;

a retimer coupled to the slicer, ~~wherein~~ the retimer being configured to generate ~~generates~~ recovered equalized data from the binary signal in response to an extracted clock signal, and

a multiplier coupled to the retimer, ~~wherein~~ the multiplier being configured to apply ~~applies~~ an equalization coefficient to the recovered equalized data to generate the equalized feedback signal; and

a clock and data recovery circuit coupled to the slicer, ~~wherein~~ the clock and data recovery circuit being configured to generate ~~generates~~ the extracted clock signal from the binary signal, [[and]] wherein the clock and data recovery circuit is configured to adjust ~~adjusts~~ phase of the extracted clock signal to compensate for processing delays in the decision feedback equalizer.

13. (Currently Amended) The communications system of claim 12 wherein the clock and data recovery circuit comprises:

a phase detector configured to generate ~~for generating~~ a phase error signal in accordance with a difference in phase of the extracted clock signal and the binary signal;

a voltage controlled oscillator configured to generate ~~for generating~~ the extracted clock signal as a function of the phase error signal; and

a delay coupled between the voltage control oscillator and the phase detector and configured to adjust ~~for adjusting~~ phase of the extracted clock signal.

14. (Currently Amended) The communications system of claim 12 wherein the clock and data recovery circuit comprises:

a phase detector configured to generate ~~for generating~~ a phase error signal in accordance with a difference in phase of the extracted clock signal and the binary signal; and

a voltage controlled oscillator configured to generate ~~for generating~~ the extracted clock signal as a function of the phase error signal, wherein the phase detector is configured to adjust ~~adjusts~~ the phase error signal in response to a phase offset signal to adjust phase of the extracted clock signal.

15. (Currently Amended) A communications system comprising:

a decision feedback equalizer adapted to reduce channel related distortion in received data, wherein the decision feedback equalizer generates equalized data; and

a clock and data recovery circuit coupled to the equalizer, wherein the clock and data recovery circuit is configured to generate~~generates~~ an extracted clock signal from the equalized data, and wherein the decision feedback equalizer includes a retimer that is configured to generate~~generates~~ recovered equalized data from the equalized data in response to the extracted clock signal; and

a real time optimizer coupled to the clock and data recovery circuit, wherein the real time optimizer is configured to generate~~generates~~ a phase adjust signal and wherein the clock and data recovery circuit is configured to adjust a ~~adjusts~~ phase of the extracted clock signal in response to the phase adjust signal to compensate for processing delays in the decision feedback equalizer.

16. (Currently Amended) The communications system of claim 15 wherein the decision feedback equalizer comprises a summer that is configured to combine ~~combines~~ an equalized feedback signal with the received data to generate the equalized data.

17. (Currently Amended) The communications system of claim 16 further comprising a monitor circuit is configured to generate~~for generating~~ a sum square error signal from the equalized data and wherein the real time optimizer is configured to adjust ~~adjusts~~ the phase adjust signal to reduce the sum square error signal.

18. (Currently Amended) The communications system of claim 17 wherein the decision feedback equalizer further comprises a slicer coupled to the summer, ~~wherein~~ the slicer being configured to convert ~~converts~~ the combined signal to a binary signal, **[[and]]** wherein the clock

and data recovery circuit is configured to generate~~generates~~ the extracted clock signal ~~having an adjustable phase offset~~ from the binary signal.

19. (Currently Amended) The communications system of claim 18 wherein the equalizer retimer comprises a flip flop coupled to the slicer and the clock and data recovery circuit and wherein the flip flop is configured to generate~~generates~~ the recovered equalized data from the binary signal in response to the extracted clock signal.

20. (Currently Amended) The communications system of claim 15 wherein the clock and data recovery circuit comprises:

a phase detector configured to generate ~~for generating~~ a phase error signal in accordance with difference in phase of the extracted clock signal and the equalized data;

a voltage controlled oscillator configured to generate ~~for generating~~ the extracted clock signal as a function of the phase error signal; and

a delay coupled between the voltage control oscillator and the phase detector configured to adjust ~~for adjusting~~ phase of the extracted clock signal.

21. (Currently Amended) The communications system of claim 15 wherein the clock and data recovery circuit comprises:

a phase detector configured to generate ~~for generating~~ a phase error signal in accordance with a difference in phase of the extracted clock signal and the equalized data; and

a voltage controlled oscillator configured to generate ~~for generating~~ the extracted clock signal as a function of the phase error signal, wherein the phase detector is configured to adjust ~~adjusts~~ the phase error signal in response to a phase offset signal to adjust phase of the extracted clock signal.

22. (Currently Amended) A method ~~of reducing channel related distortion in received data~~ comprising:

providing received data to a decision feedback equalizer;

generating, by the decision feedback equalizer, a binary signal according to the received data;

generating a phase delay signal based on processing delays associated with the decision feedback equalizer;

extracting a clock signal from the binary signal according to the phase delay signal, to thereby compensate for the processing delays; and

retiming the binary signal according to the clock signal.

23. (Currently Amended) The method of claim 22 wherein a real time optimizer generates the phase delay signal based on an amount of channel-induced distortion associated with the received data.

24. (Currently Amended) The method of claim 22 wherein generating the phase delay signal comprises delaying [[a]] the clock signal output from a voltage control oscillator to a phase detector receiving the binary signal.

25. (Currently Amended) The method of claim 22 wherein generating the phase delay signal comprises:

generating a distortion error signal in accordance with a soft decision signal generated by the decision feedback equalizer.

26. (Currently Amended) The method of claim 25 wherein generating the phase delay signal comprises generating ~~a real time optimizer generates~~ the phase delay signal by processing the distortion error signal.